UNIVERSITY COLLEGE OF ENGINEERING
OSMANIA UNIVERSITY, HYDERABAD
M. E. (ECE, Mech. & CSE) I - Semesters (Main) Examination
January/February 2018
MVSR ENGINEERING COLLEGE
RE-REVISED EXAMINATION TIME TABLE

TIME : 2.00 PM TO 5.00 PM

DATE & DAY	E. C. E. (EMBEDDED SYSTEMS & VLSI DESIGN)	MECHANICAL (CAD / CAM)	C. S. E.
	I-Semester	I-Semester	I-Semester
18-01-2018 THURSDAY	Analog IC Design	Product Design and Process Planning	Advanced Algorithms
20-01-2018 SATURDAY	Digital Signal Processors	Failure Analysis and Design	Artificial Intelligence
22-01-2018 MONDAY	Global & Regional Navigational Satellite Systems	=====	=====
24-01-2018 WEDNESDAY	Micro Controllers for Embedded System Design	Computer Integrated Manufacturing	Advanced Operating Systems
27-01-2018 SATURDAY	VLSI Design & Technology	Finite Element Techniques	Object Oriented Software Engineering
29-01-2018 MONDAY	Advanced Digital Design with Verilog HDL	Optimization Techniques	Software Quality Testing
31-01-2018 WEDNESDAY	=====	Experimental Techniques and Data Analysis	Mobile Computing

DIRECTOR OF EVALUATION
EXAMINATION CELL